**Techninis ir istorinis kontekstas:**

Z80000:

Zilog Z80000 yra neišleistas 32 bitų procesorius pagamintas 1986 metais. Ši architektūra buvo pagaminta praplėčiant 16 bitų Zilog Z8000 turinti daugiaprocesorinį pajėgumą, šešių etapų komandų vykdymo konvejerį ir 256 baitų spartinančią atmintį. Gali adresuoti iki 4 GB RAM atminties, tačiau negali vykdyti kodo parašyto Z8000 arba Z80 procesoriams. Procesorius daugeliu atžvilgių yra panašus į „Intel“ 80386. Dėl pradinės gamybos vėlavimo Z80000 pasiekė tik bandomasis testavimo etapas, niekada nebuvo nepaleistas komerciškai.

PA-RISC (Precision Architecture [RISC](https://en.wikipedia.org/wiki/Reduced_instruction_set_computer)) architektūra buvo pagaminta [Hewlett-Packard](https://en.wikipedia.org/wiki/Hewlett-Packard) kompanijos 1986 metais. Pagal šią architektūrą pagamintos sistemos buvo pardavinėjamos iki 2008 metų, tačiau iki 2013 metų palaikė serverius, kuriuose veikia PA-RISC lustai. Pagal PA-RISC architektūrą buvo sukurtas Intel Itanium procesorius.

PA-RISC is Hewlett Packard’s Reduced Instruction Set Computing (RISC) architecture developed in the 1980s and used until the mid-2000s in Unix and industrial HP computers. The computers covered on this site, the [HP 9000](https://www.openpa.net/systems/), are based on the Precision Architecture and [PA-RISC processors](https://www.openpa.net/pa-risc_processors.html) and used custom HP system designs.

**Kompiuterio/procesoriaus bazė:**

* **Technology:** Integrated Circuits (ICs)
* **Integration Scale:** **Large Scale Integration (LSI)**. This refers to the integration of thousands of transistors on a single chip.
* **Transistors:** It used **metal-oxide-semiconductor (MOS)** technology, which was common in the late 1970s and early 1980s.

**Architektūra:**

Z80000 procesorius turi šešiolika 32 bitų registrų. Komandų sistemoje yra 9 adresavimo būdai, operacijos su bitais, bitų laukais, baitais, žodžiais (16 bitų), ilgais žodžiais (32 bitų) ir kintančio ilgio tekstinėmis eilutėmis (iki 65,536 baitų) . The memory management, exception handling, and system and normal mode features support the development of reliable software systems.

**Kokių adresų mašinos:**

PA-RISC the typical execution data flow consists of reading two operands from general-purpose registers, routing these two operands through the ALU or the SMU with the proper function selected, and storing the result back into a general register. This is the data flow for the basic three-register model of execution, which facilitates single-cycle execu tion, since no memory references are required.

**Registrai:**

Z80000 procesorius turėjo šešiolika 32 bitų fizinių registrų, kurie buvo pagaminti praplėčiant 16 bitų Z8000 procesorių, kurie tapo registrų dalimi. Šioje architektūroje buvo galima pasiekti ir 16 bitų, ir 8 bitų registrus, esančius viduje 32 bitų registrų, taip pat galima buvo sujungti du registrus ir tada procesorius interpretuodavo juos kaip aštuonis 64 bitų registrus.

Bendro naudojimo registrai talpina 64 baitus atminties.

Pirmi 16 baitų (RL0, RH0, ..., RL7, RH7) naudojami kaip akumuliatoriai baitų ilgio duomenims. Pirmi 16 žodžių registrai (R0, R1, ..., R15) naudojami kaip akumuliatoriai žodžių ilgio duomenims, kaip indeksavimo registrai (išskyrus R0), arba atminties adresams in compact mode. Bet kuris ilgo žodžio registras (RR0, RR2, ..., RR30) gali būti naudojamas skaičiavimas su ilgais žožiais, arba kaip indeksų registras (išskyrus R0) in segmented or linear mode or for memory addresses. 64 bitų registrai (RQ0,RQ4, ..., RQ28) gali būti naudojami kaip akumuliatoriai dauginimui, dalinimui ir ženklo praplėtimui. Within quadword register RQn, RRn contains the more significant longword. A 4-bit field in instructions specifies which general purpose register to access. The register size is determined by the instruction opcode.

PA-RISC turėjo 32 32-bitų bendros paskirties registrus.

Nulinis registrass visada gražina nulį, ir kai į jį rašome, reikšmė vistiek išlieka nulis.

25 valdymo registrus, kurie yra naudojami virtualių adresųų apsaugojimui, pertraukimų apdorojimui ir įvairioms funkcijoms.

8 erdvės registrai naudojami sukurti virtualiems adresams.

**Požymių bitai:**

Z80000 architektūroje buvo naudojami šeši požymių bitai: pernešimo (C), nulio (Z), ženklo (S), lyginumo/perpildymo (P/V), Decimal Adjust (D)- yra naudojamas BCD (binary coded decimal) skaičiavimuose, kad sekti, koks paskutinis veiksmas buvo atliktas – sudėtis ar atimtis. Half Carry (H) – taip pat yra naudojamas BCD (binary coded decimal) , kad paversti rezultatą iš buvusios atimties ar sudėties į dešimtainį skaičių.

**Mašininis žodis**

Abiejų architektūrų mašininio žodžio plotis buvo 32 bitų.

**Atminties išdėstymas, adresų erdvė, efektyvus adreso plotis, maksimalus įmanomas atminties kiekis, tipiškas atminties kiekis**

Z80000

Z80000 procesorius turėjo tris adresavimo būdus: (nuo 20psl jei truks info)

* Compact – naudojamas tų programų, kurių adresų erdvė yra mažesnė nei 64Kb ir gali efektyviai naudoti 16-bitų adresus
* Segmented – palaiko 2 segmentavimo dydžius – 64Kb ir 16Mb. In segmented mode, address calculations do not affect the segment number, only the offset wi thin the segment. 32,768 segments of 64 KB (16-bit address; comprising memory from 0-2GB) *and* 128 segments of 16 MB (24-bit address; comprising memory from 2GB-4GB), making a total of 4 GB (32-bit address) of accessible memory.
* Linear - The 32-bit addresses in linear mode provide uni form and unstructured access to 4G bytes of memory. Some applications benefit from the flexibil ity of linear addressing by allocating objects to arbitrary positions in the address space

Kurie buvo parenkami pagal valdymo bitus požymių bitų ir valdymo žodžio registruose.

PA-RISC HP Precision processors access memory using byte ad dresses. Larger addressable units include half words, words, and double words. An address is either physical or virtual. All load and store instructions can be used in either virtual or physical mode. Virtual mode is enabled sepa rately for instruction fetches and data accesses by two flags in the processor status word. A pointer to physical memory is a 32-bit unsigned integer whose value is the address of the first byte of the operand it designates. Physical addresses are used directly, with no protection or access rights checking performed. Virtual ad dresses are translated to physical addresses and undergo protection and access rights checking as part of the trans lation. This allows the hardware support for access control to be built into the storage unit.

**Virtuali atmintis:** Z80000 architektūroje virtualioji atmintis buvo palaikoma puslapiavimu.

Another memory management function, demand-paged v irtual memory, a !lows programs to execute even when only a portion of their memory requirements is available in primary storage. The rest of the program can be stored in secondary storage, typi cally on disk. Thus, virtual memory improves a system's cost/performance by permitting programs to execute with varying amounts of memory.

The CPU implements a paged translation mechanism similar to that of most mainframe and super-mini computers. The operating system creates transla tion tables in memory, then loads pointers to the tables in control registers. The CPU automatically refers to the tables to perform address transla tion and access protection. To manage the large logical address space, the translation scheme divides it into fixed-size, 1K byte pages.

PA-RISC architektūroje yra trys lygiai, jie priklauso nuo to, kiek virtualios atminties yra palaikoma.

0-nis lygis nepalaiko jokios virtualios atminties. Pirmo lygio procesorius plaaiko 16-bitų erdvės registrus skirtus 48 bitų virtualios atminties erdvei ir trečio lygio procesorius įgyvendina 32-bitų erdvės registrus kur palaikoma pilna 64 bitų virtuali adresų erdvė.

**Komandų sistema:** Z80000 architektūros komandų sistema turėjo apie 800 skirtingų komandų. Turėjo 11 instrukcijų klasių:

* Load and Exchange,
* Aritmetinės(Arithmetic)
* Loginės (Logical)
* Programos valdymo (Program Control)
* Veiksmų su bitais (Bit Manipulation)
* Rotate and Shift, blokų perkėlimo ir komandos su tekstinėmis eilutėmis (Block Transfer and String Manipulation)
* Įvesties ir išvesties (Input/Output)
* Procesoriaus valdymo (CPU Control)
* Papildomos instrukcijos (Extended Instructions).

PA-RISC turėjo 140 komandų. Jos yra išskirstytos į šias klases:

* FLOP – operacijos su slankaus kablelio skaičiais
* LDST – komandos darbui su atmintim – (load and store)
* ALU – veiksmai su sveikais skaičiais (integer ALU)
* MM – (shifts, extracts, deposits)
* NUL - Might nullify successor
* BV – branch vectored local, branch external
* BR – other branches
* FSYS – FTEST and FP status/exception
* SYS – system control instructions

In HP Precision Architecture, all instructions have a fixed length of thirty-two bits, which is one word of memory. Time-critical functions are placed in fixed-position fields, so that they can proceed with minimal or no decoding. Since all instructions are word-aligned, an instruction never crosses a page boundary.

**Adresavimo būdai:**

Z80000The CPU locetes operands (the data manipulated by inatructions) in regiaters, memory, peripheral ports, or in the inatruction. The location of an operand is specified by one of nine general addresaing modes: Register, Immediate, Indirect Register, Direct Address, Index, Baae Addresa, Base Index, Relative Address, and Relative Index. Instruction formats provide compact encodinga for the most frequently used addressing modes.

PA-RISC turėjo tik tris adresavimo būdus - long/short displacement and indexed

**I/O galimybės**

Z80000 Al though logical I/O addresses are 32 bits, only the 16 low-order bits of a logical I/O address can be manipulated; the CPU always forces the 16 high order bits to O. Unlike logical memory address spaces, logical I/O address space is not viewed as a string of bytes at consecutive addresses. Rather, the address is simply used to locate a byte, word, or longword peripheral port. The byte port located at address n does not have to be contiguous with the byte port located at address n+1, nor must it be the more significant byte of the word port located at address n. Logical I/O addresses can be either even or odd.

PA-RISC The input/output (I/O) architecture is memory mapped. That is, complete control of all system components (of which I/O attachments are a special case) is exercised by the execution of load and store instructions to virtual or physical addresses. This approach permits I/O drivers to be written in high-level languages. Furthermore, since the usual page-level protection mechanism is applied during virtual-to-physical address translation, user programs can be granted direct control over particular I/O devices with out compromising system integrity.

**Pertraukimai**

The Z80,000 palaiko tris pertraukimų rūšis:

* neužmaskuojamas (nonmaskable) -
* vektorinius (vectored)
* nevektorinius (nonvectored).

Neužmaskuojamas pertraukimas – aukščiausio prioriteto, yra rezervuojamas kritiniams atvejams, tokiem kaip staigus energijos nutrūkimas. Vektoriniai ir nevektoriniai pertraukimai gali būti paslepiami su požymių bitais valdymo žodžio registre. Vektoriniai pertraukimai leidžia iššakoti pertraukimą į atskirą išimčių tvarkyklę, parinktą kode. Ne vektoriniai pertraukimai naudoja paprastą pertraukimų tvarkyklę.

PA-RISC

The architecture implements a single-level interruption system. This means that once an interruption is chosen for service, it cannot be preempted for service by a higher- priority interruption. It also implies that only one interrup tion is serviced at a time. If an instruction raises multiple interruptions, the highest-priority interruption is serviced, and then the instruction is reexecuted, which causes the other interruptions to be raised again. Then the next high est-priority interruption is serviced, and so on. The nesting of interruptions is not excluded, since the interruption handling routine can choose to reenable other interruptions once it has saved the appropriate state. Since the machine state is saved in registers rather than in mem ory when an interruption is serviced, interruption handlers must leave interruptions disabled until they have saved the machine state in memory. In certain pipelined processors, interruptions are often not precise, in the sense that they may not be serviced immediately after the instruction that caused the interrup tion. This is because in overlapped instruction processing, several successive instructions may already have been par tially or fully processed by the time the interruption caused by an instruction is generated. This imprecision adds con siderable complexity to interrupt handling routines.

**Duomenų tipai:** Z80000 procsorius palaikė komandas su 9 duomenų tipais: bitais, bitų laukais, sveikais skaičiais su ženklu, sveikais skaičiais be ženklo, loginėmis reikšmėmis, adresais, BCD (dvejetaine skaičiavimo sistema užkoduotas dešimtainis skaičius), stecke esančiomis reikšmėmis, tekstinėmis eilutėmis. Sveikas skaičius ir loginės reikšmės gali būti baito, žodžio, ar ilgo žodžio dydžio. Veiksmai su slankaus kablelio skaičiais yra įgyvendinami Extended Processing Architec ture (EPA) facility by a coproceasor (ZB07D Arith metic Processing Unit) or by software emulation. Yra galimybė atlikti veiksmus su trupmeniniais skaičiais remiantis Support is provided for Binary Coded Decimal (BCD) arith metic and multiple precision arithmetic.

PA-RISC

Sveiki skaičiai su ženklu ar be ženklo gali būti 8, 16 arba 32 bitų ilgio. Skaičiai su ženklu įgyvendinami papildinio iki dviejų logika abiejose architektūrose. Simboliai yra 8 bitų ilgio ir palaiko ASCII standartą. Slankaus kablelio skaičiai yra saugomi 32 arba 64 bitų ilgio, kurie palaiko ANSI/IEEE 754-1985 standartą. BCD irgi..

**Sistemos greitaveika:**

Z80000 The system designer can fine-tune performance by selecting not only the CPU clock rate and bus speed (1/2 or 1/4 the CPU clock), but also the access time and date path width for the memory. for two independent regions of memory the CPU can be programmed for both the number of wait states automatically inserted, and whether the data path is 16 or 32 bits wide. With these options, a system can essily accommodate slow, 16-bit-wide bootstrap read-only memory (ROM) in one region and fast, 32-bit-wide random access memory (RAM) in the other. furthermore, the CPU supports an optional burst transfer of several memory words from consecutive locations. Burst transfers can increase memory bandwidth for interleaved and "nibble-mode" memory systems.

PA-RISC - A primary design goal was that all functional computa tions in the basic instruction set could execute in one machine cycle in a pipelined implementation of the proces sor architecture. Operations were selected for inclusion in the basic instruction set only if they could be implemented in a reasonably small number of logic levels, to guarantee a short cycle time. This does not necessarily mean that the operation performed had to be primitive in function. In fact, rather sophisticated operations were allowed in the architecture if they proved useful to the compilers, and were implementable in a short machine cycle with rela tively simple hardware. ively simple hardware. Complex operations that are necessary to support re quired software functions but cannot be implemented in a single execution cycle are broken down into primitive op erations, each of which can be executed in a single cycle. Single-cycle execution was a design goal of the architec ture, but is not a constraint on the implementations. For example, an HP Precision microprocessor may operate with slower memories, performing a load instruction in more than one cycle.

**Spartinančioji atmintis**: Z80000 įgyvendina spartinančios atminties mechanizmą, kuri laiko kopiją neseniai naudotos atminties vietos/adreso (location) on-chip. Tose vietose laikomos ir instrukcijos, ir duomenys. Kai bandoma pasiekti atmintį, procesorius patikrina, galbūt tai ko ieškome yra spartinančioje atmintyje. Jeigu neranda, perkopijuoja tą informaciją iš atminties į spartinančiąją atmintį vietoj seniausiai naudotų duomenų. Taip sumažinama atminties skaitymo operacijų. 256 baitų dydžio. The cache stores copies of inetruction and data memory locstione. Instructions are read from the cache on the instruction bus. Data is read from or written to the cache on the memory bus. The Translation Lookaside Buffer (TLB) trans lates logical addresses calculated by the address arithmetic unit to physical addresses used to access the cache.

PA-RISC

A virtual address is defined globally and has the same meaning when used by any process. This is in contrast to other architectures, which permit use of the same address for different objects by different processes. The virtual ad dress space is so large that processes can be assigned sepa rate address ranges for private data. Address translation information does not need to change upon a process switch and the information needed for address translation can be represented more compactly. Global virtual addressing therefore allows closely coupled processes to accumulate a stable working set of address translations in spite of fre quent process switching.

Virtual memory is structured as a set of address spaces, each containing 2^32 bytes. A level-one processor imple ments 2^16 spaces (16-bit space registers), and a level-two processor implements 2^32 spaces (32-bit space registers). A space is specified by a space identifier, and is divided into pages, each 2048 bytes in length. For a level-two processor, the concatenation of a 32-bit space identifier and a 32-bit offset within the space forms a virtual address. Alternatively, a virtual address may be viewed as the concatenation of a 53-bit virtual page number and an 11 -bit offset within the page. For virtual addressing, space identifiers are specified in space addressing registers. These include the space portion of the instruction address register and the eight space regis ters SR 0 through SR 7 (see Fig. 4). One such register is implicitly or explicitly selected by every instruction that generates a virtual address. (jei truks info tai 14 psl)

**Kur buvo naudojamos:**

The regular combination of addressing modes, operations, and data types offers a powerful instruction set that is well-suited for compila tion of high-level languages such as C, Pascal, and Ada. Z80000

**Kiek programinės įrangos parašyta:**

Z8000 COMPATIBILITY The 180,000 CPU's instruction set encoding allows it to directly execute Z8000 family software such as compilers and the 1RTS~ real-time operating system. Z8000 programs must not use the 18000 privileged instructions, address, and control field encodings if they are to execute correctly on the Z80,000 CPU, since the Z80,000 CPU uses many of these reserved encodings to extend the register file, address range, and instruction functionali t y.

**Šaltiniai:**

<https://en.wikipedia.org/wiki/Zilog_Z80000>

<https://www.openpa.net/pa-risc_architecture.html>